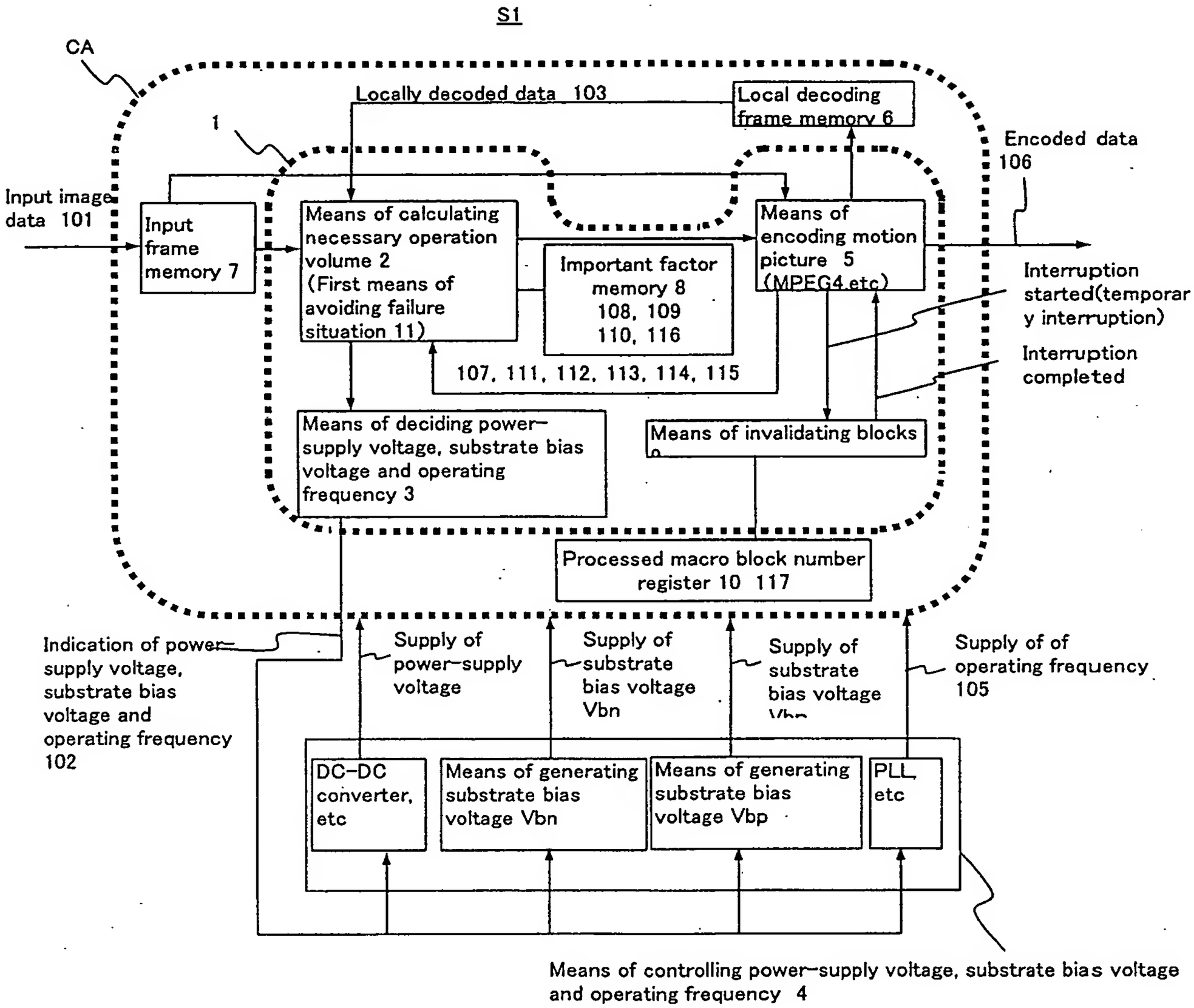
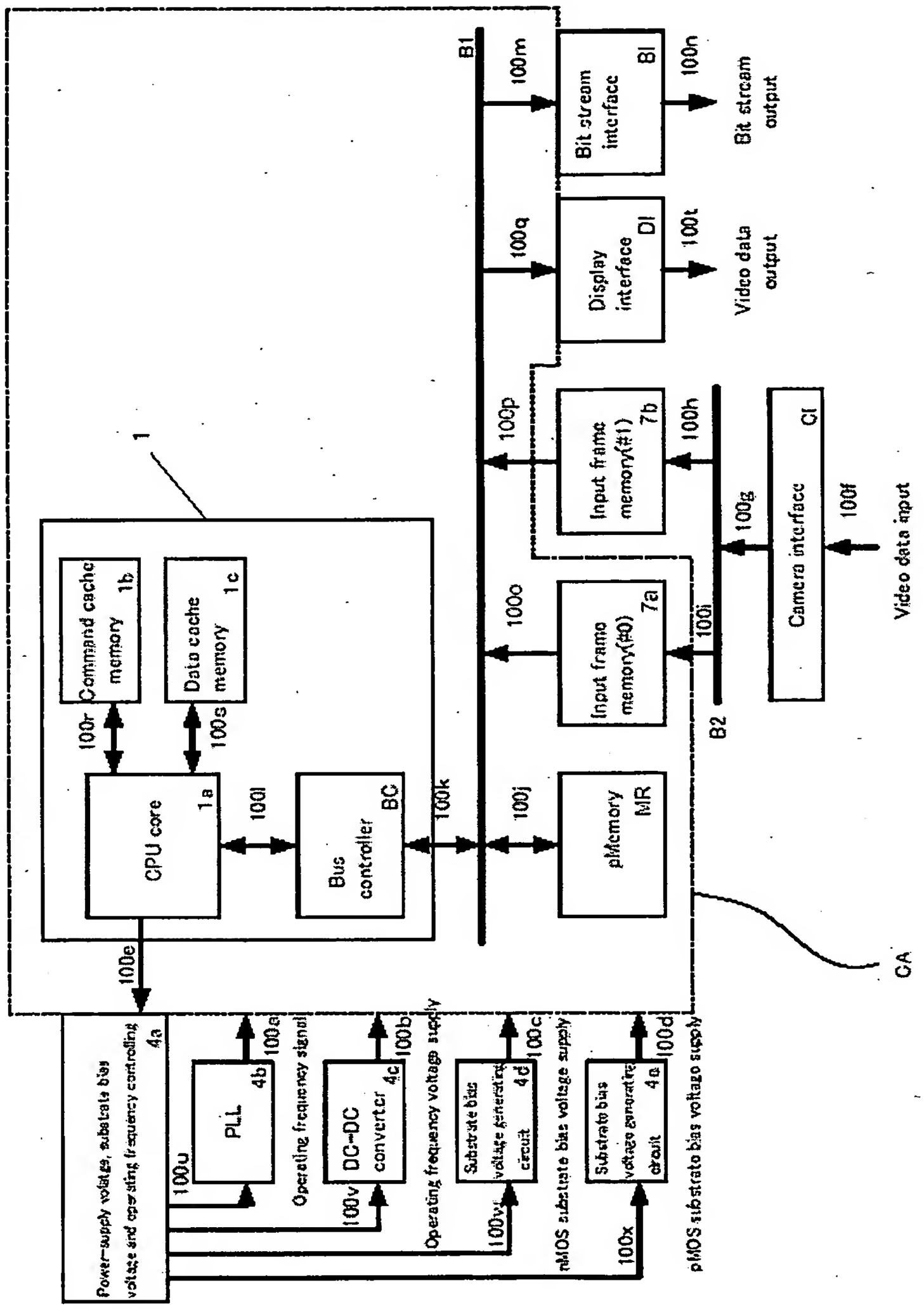
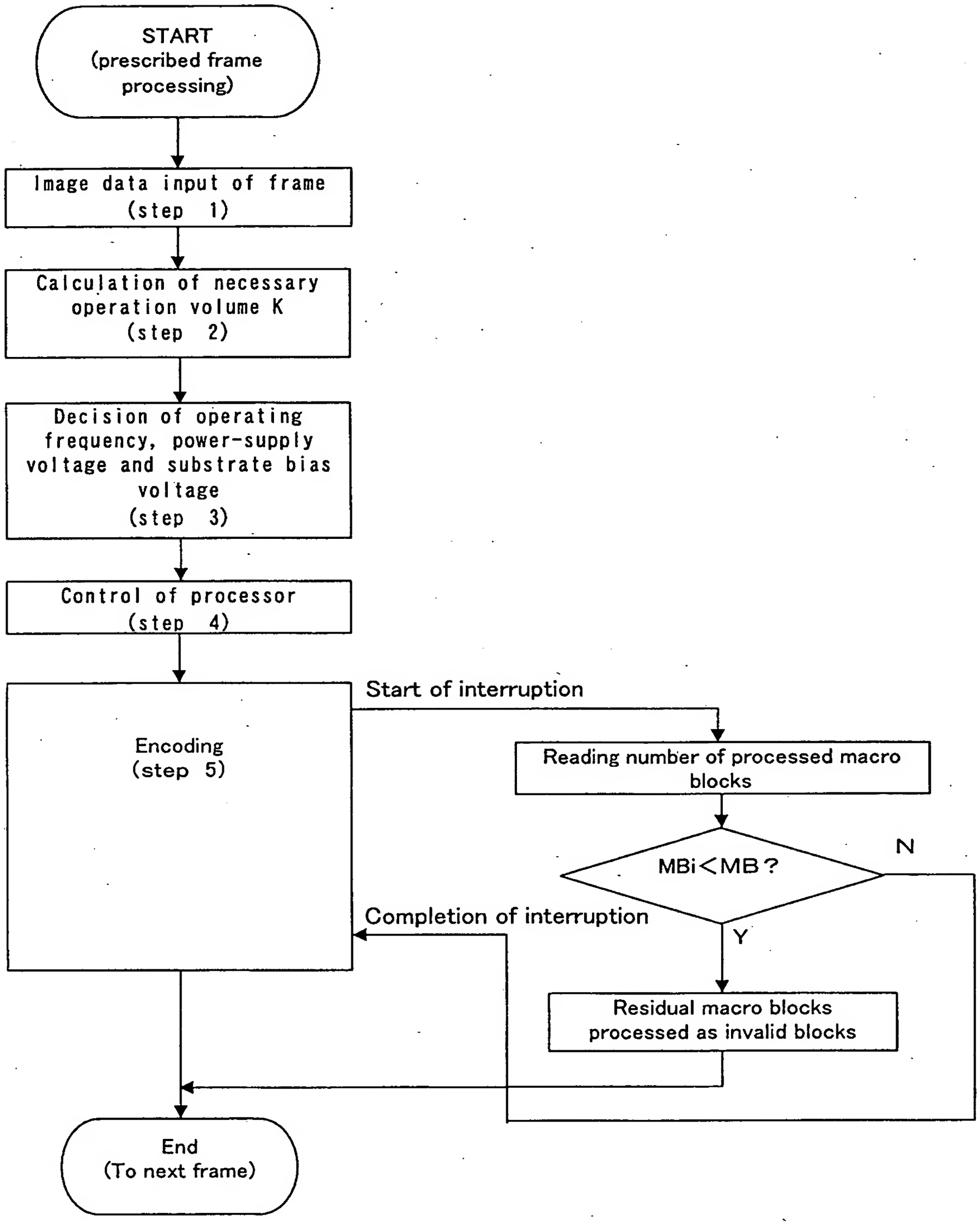
【Fig1】


S1
CA
1
Locally decoded data 103
Local decoding frame memory 6
Encoded data 106
Input image data 101
Input frame memory 7
Means of calculating necessary operation volume 2 (First means of avoiding failure situation 11)
Important factor memory 8 108, 109 110, 116
Means of encoding motion picture 5 (MPEG4 etc)
Interruption started(temporary interruption)
Interruption completed
107, 111, 112, 113, 114, 115
Means of deciding power-supply voltage, substrate bias voltage and operating frequency 3
Means of invalidating blocks
Processed macro block number register 10 117
Indication of power-supply voltage, substrate bias voltage and operating frequency 102
Supply of power-supply voltage
Supply of substrate bias voltage Vbn
Supply of substrate bias voltage
Supply of of operating frequency 105
DC-DC converter, etc
Means of generating substrate bias voltage Vbn
Means of generating substrate bias voltage Vbp
PLL, etc
Means of controlling power-supply voltage, substrate bias voltage and operating frequency 4

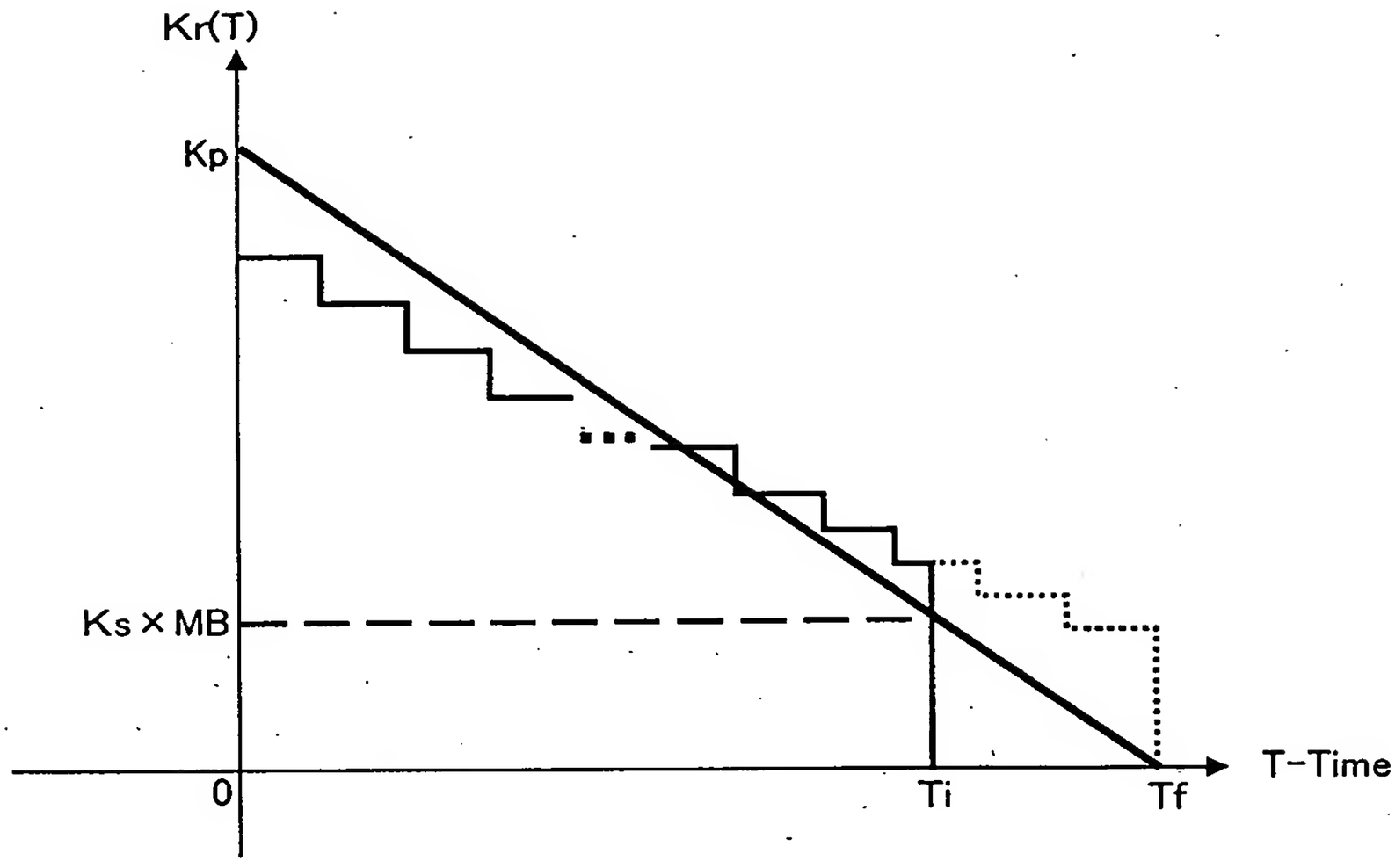
【Fig2】


B1
100m
Bit stream interface
BI
100n
Bit stream output
100q
Display interface
DI
100t
Video data output
1
Command cache memory
1b
Data cache memory
1c
100r
100s
CPU core
1a
100l
Bus controller
BC
100k
100e
100p
Input frame memory(#1)
7b
100h
100o
Input frame memory(#0)
7a
100i
100j
pMemory
MR
B2
100g
Camera interface
CI
100f
Video data input
CA
Power-supply voltage, substrate bias voltage and operating frequency controlling
4a
100u
PLL
4b
100a
Operating frequency signal
100v
DC-DC converter
4c
100b
Operating frequency voltage supply
100w
Substrate bias voltage generating circuit
4d
100c
nMOS substrate bias voltage supply
100x
Substrate bias voltage generating circuit
4e
100d
pMOS substrate bias voltage supply

【Fig3】


START
(prescribed frame processing)
Image data input of frame
(step 1)
Calculation of necessary operation volume K
(step 2)
Decision of operating frequency, power-supply voltage and substrate bias voltage
(step 3)
Control of processor
(step 4)
Encoding
(step 5)
Start of interruption
Reading number of processed macro blocks
MBi<MB?
N
Y
Completion of interruption
Residual macro blocks processed as invalid blocks
End
(To next frame)

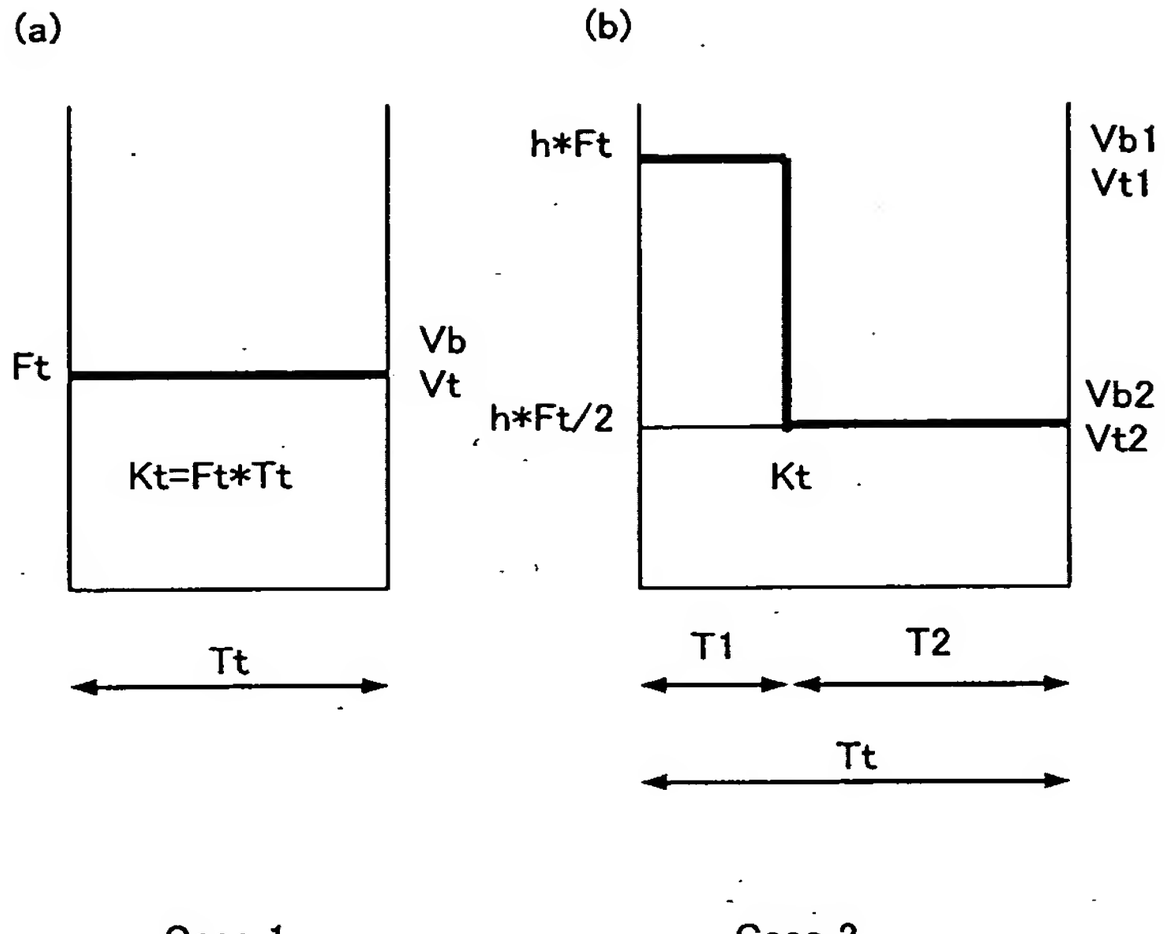
【Fig4】



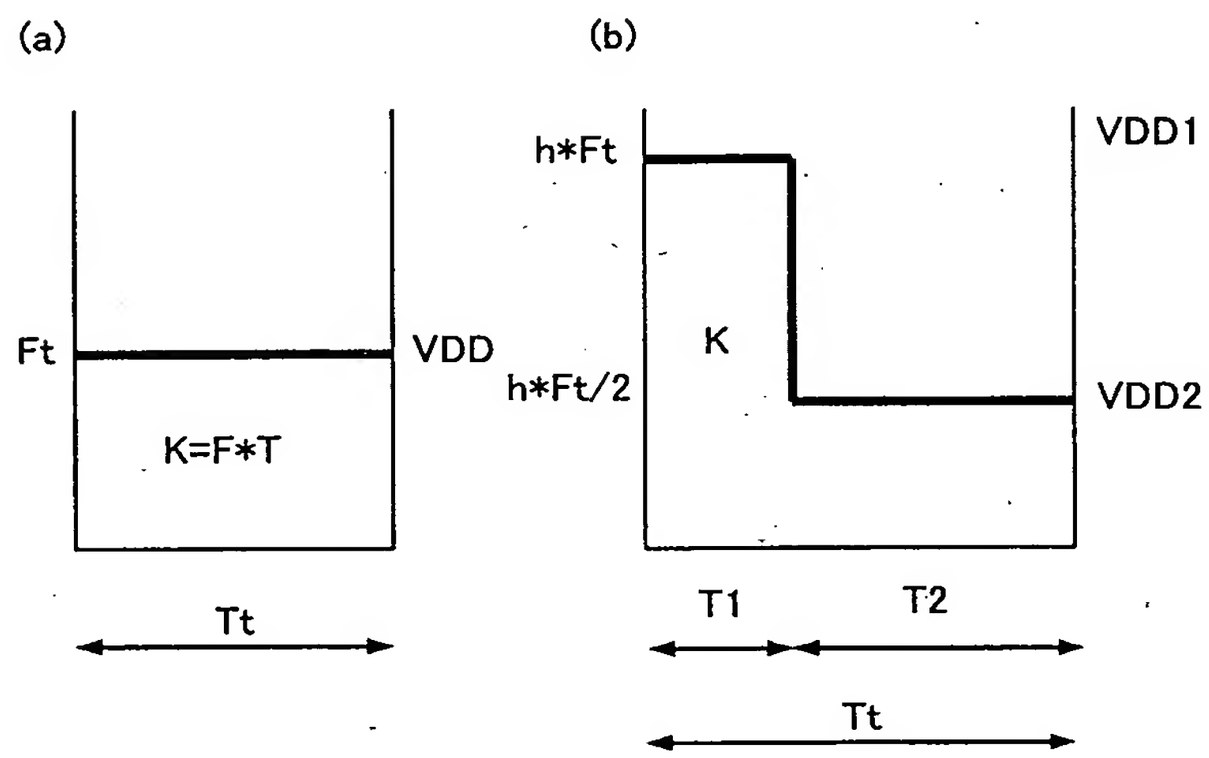
【Fig5】

Operating frequency (cycles／second)	Power-supply voltage (VDD)	Substrate bias voltage of n-channel MOS transistor (Vbn)	Substrate bias voltage of p-channel MOS transistor (Vbp)
f (1)	VDD (1)	Vbn (1)	Vbp (1)
f (2) (>f (1))	VDD (2)	Vbn (2)	Vbp (2)
f (3) (>f (2))	VDD (3)	Vbn (3)	Vbp (3)
.	.	.	.
f (n) (>f (n−1))	VDD (n)	Vbn (n)	Vbp (n)
.	.	.	.
f (r) (>f (r−1))	VDD (r)	Vbn (r)	Vbp (r)

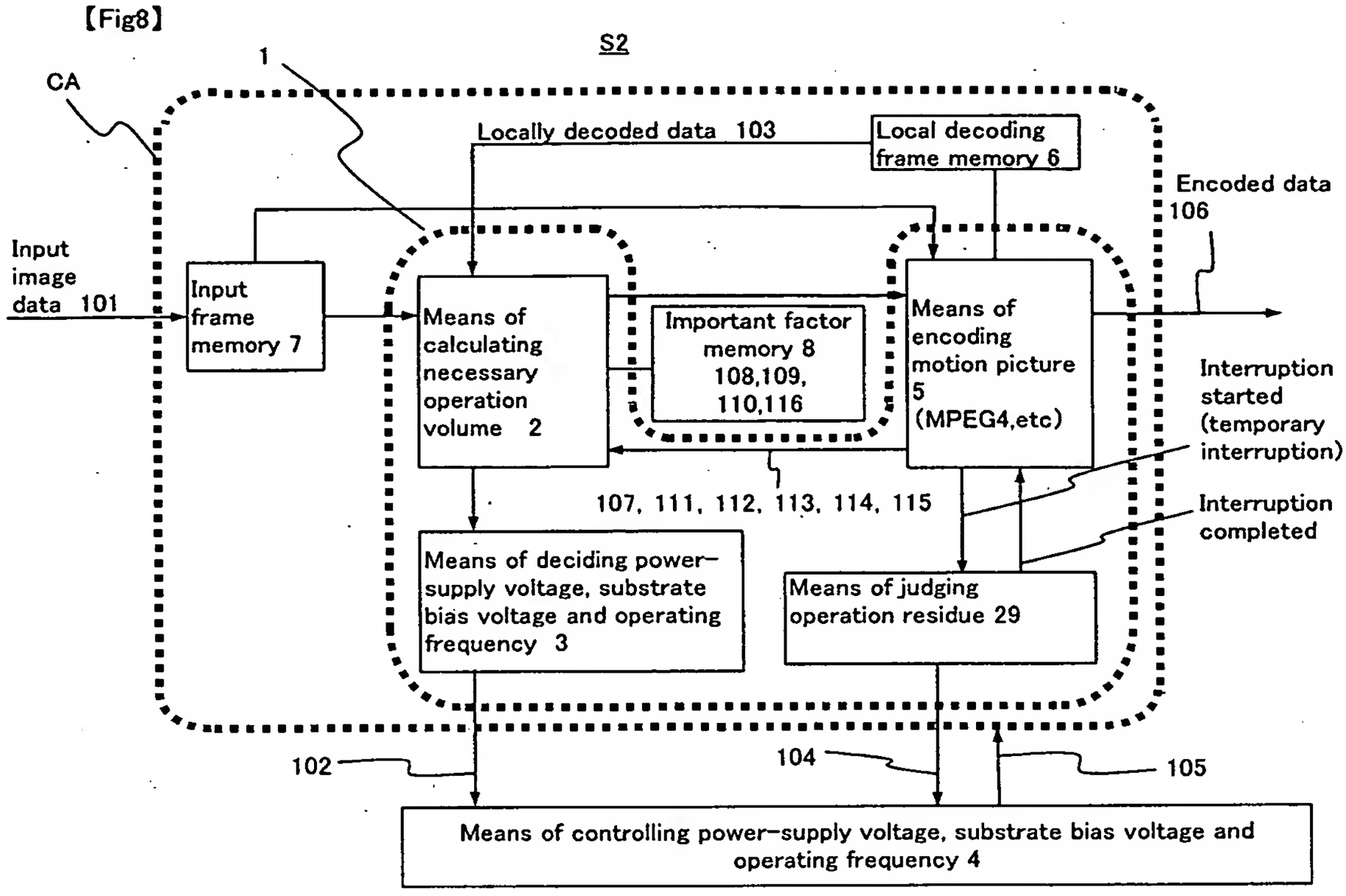
【Fig6】


(a)
(b)
Ft
Vb
Vt
Kt=Ft*Tt
Tt
h*Ft
h*Ft/2
Vb1
Vt1
Vb2
Vt2
Kt
T1
T2
Tt
Case 1
Case 2

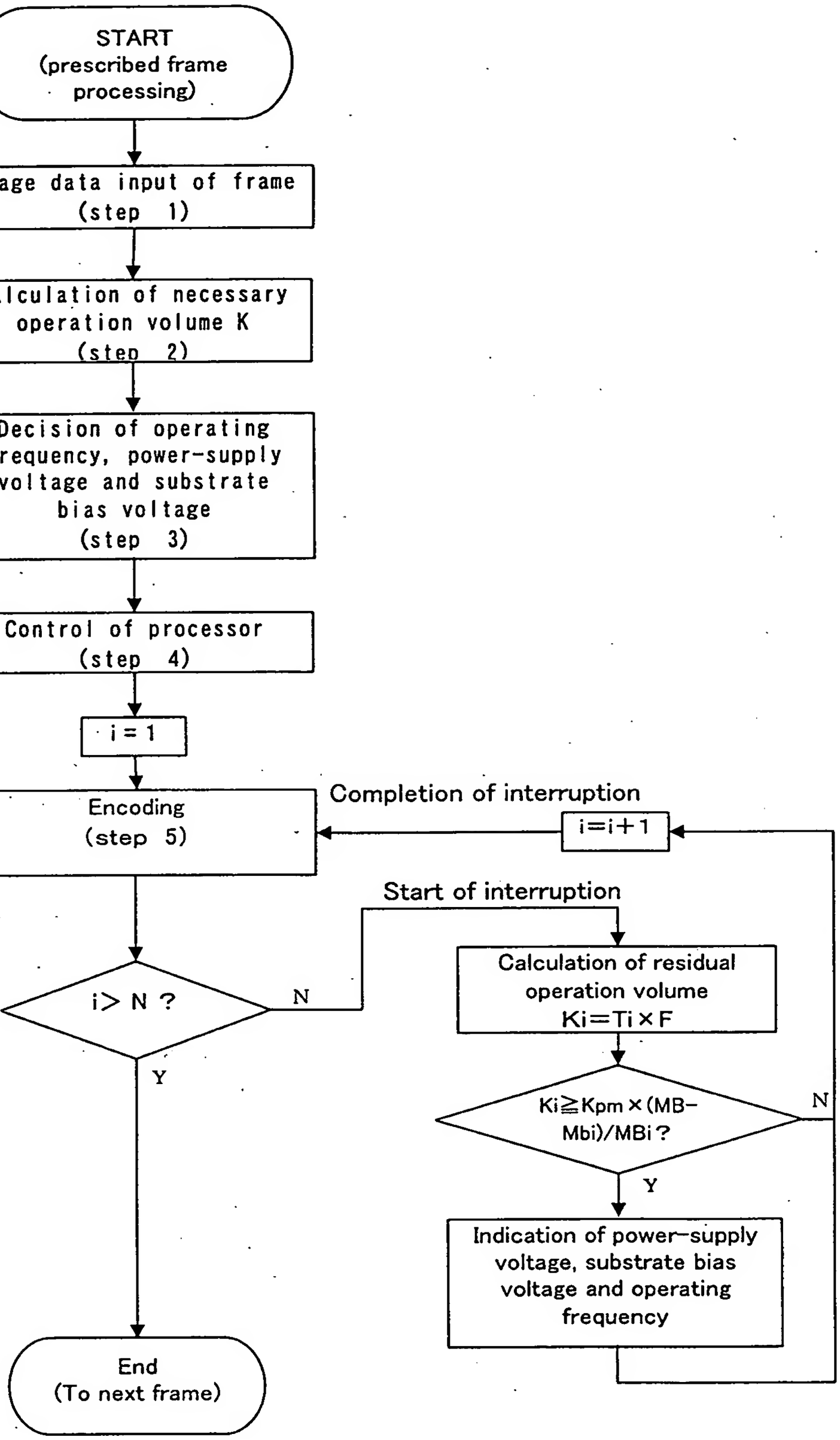
【Fig7】


(a)
(b)
Ft
VDD
K=F*T
Tt
h*Ft
h*Ft/2
K
VDD1
VDD2
T1
T2
Tt
Case 1
Case 2

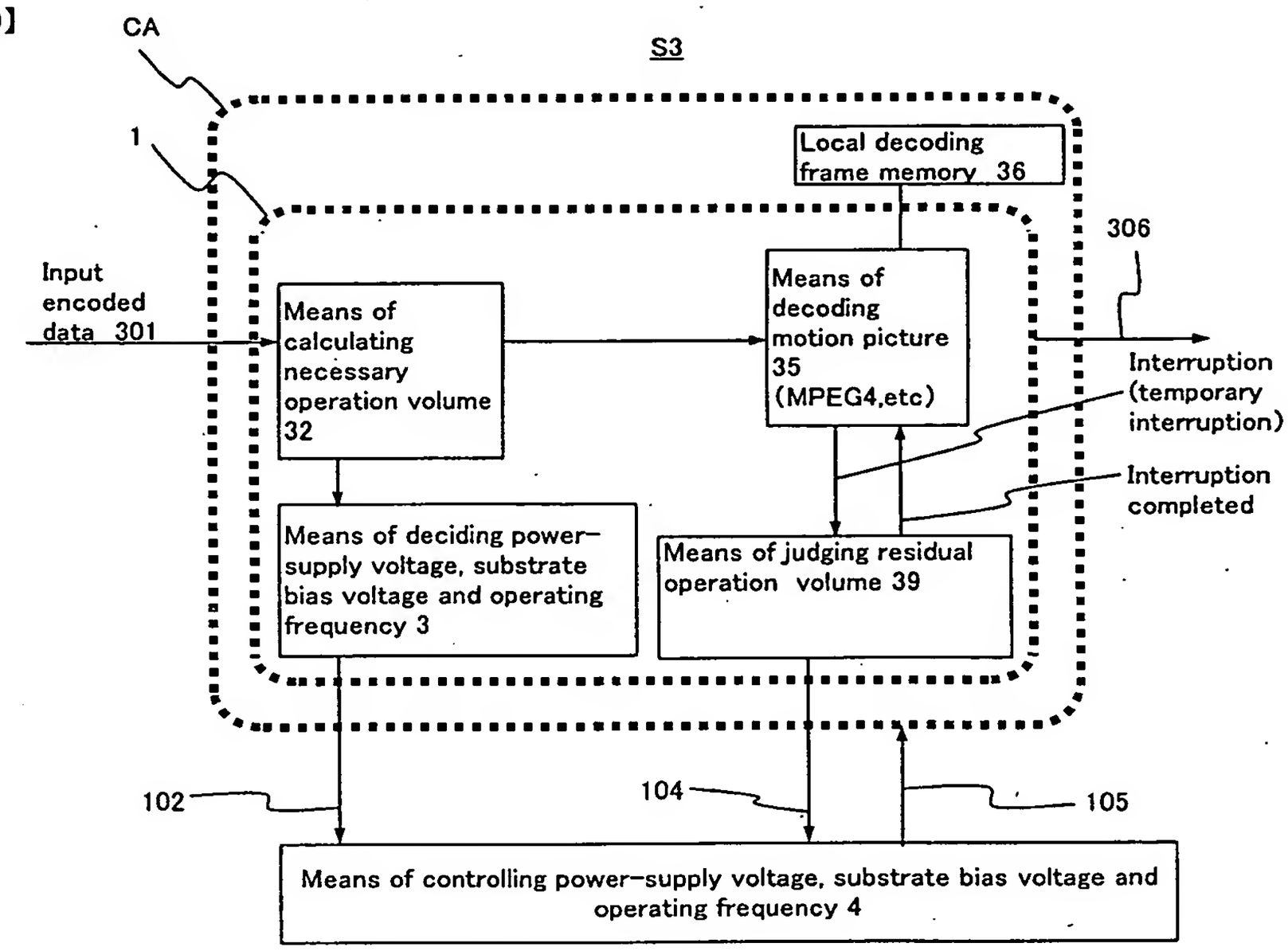
【Fig8】


S2
1
CA
Locally decoded data 103
Local decoding frame memory 6
Encoded data 106
Input image data 101
Input frame memory 7
Means of calculating necessary operation volume 2
Important factor memory 8 108,109, 110,116
Means of encoding motion picture 5 (MPEG4,etc)
Interruption started (temporary interruption)
107, 111, 112, 113, 114, 115
Interruption completed
Means of deciding power-supply voltage, substrate bias voltage and operating frequency 3
Means of judging operation residue 29
102
104
105
Means of controlling power-supply voltage, substrate bias voltage and operating frequency 4

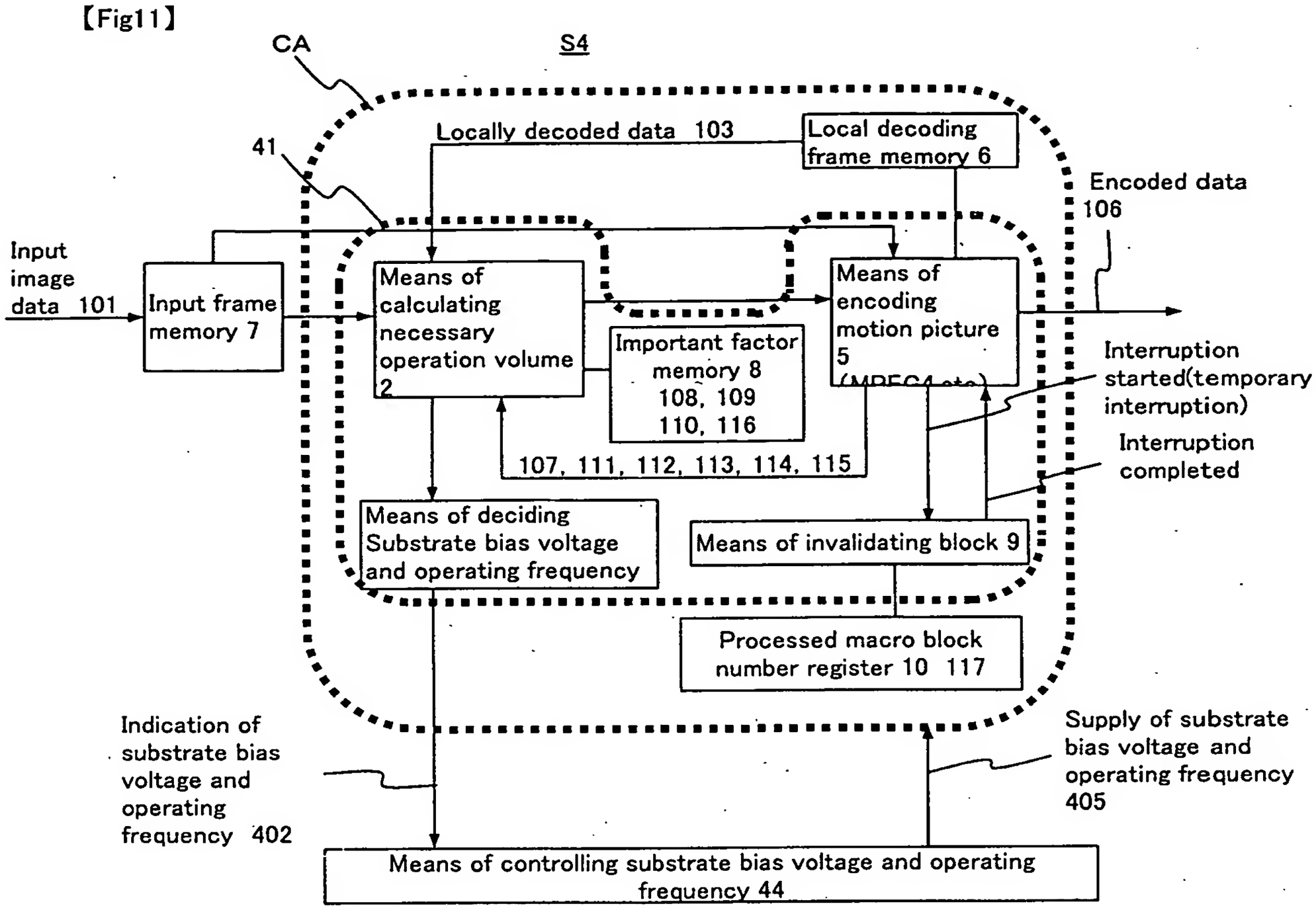
【Fig9】


START
(prescribed frame processing)
Image data input of frame
(step 1)
Calculation of necessary operation volume K
(step 2)
Decision of operating frequency, power-supply voltage and substrate bias voltage
(step 3)
Control of processor
(step 4)
i = 1
Encoding
(step 5)
Completion of interruption
i=i+1
Start of interruption
i> N ?
N
Y
Calculation of residual operation volume
Ki=Ti×F
Ki≧Kpm×(MB-Mbi)/MBi ?
N
Y
Indication of power-supply voltage, substrate bias voltage and operating frequency
End
(To next frame)

【Fig10】


CA
S3
1
Local decoding frame memory 36
306
Input encoded data 301
Means of calculating necessary operation volume 32
Means of decoding motion picture 35 (MPEG4,etc)
Interruption (temporary interruption)
Interruption completed
Means of deciding power-supply voltage, substrate bias voltage and operating frequency 3
Means of judging residual operation volume 39
102
104
105
Means of controlling power-supply voltage, substrate bias voltage and operating frequency 4

【Fig11】


CA
S4
41
Locally decoded data 103
Local decoding frame memory 6
Encoded data 106
Input image data 101
Input frame memory 7
Means of calculating necessary operation volume 2
Important factor memory 8 108, 109 110, 116
Means of encoding motion picture 5
Interruption started(temporary interruption)
Interruption completed
107, 111, 112, 113, 114, 115
Means of deciding Substrate bias voltage and operating frequency
Means of invalidating block 9
Processed macro block number register 10 117
Indication of substrate bias voltage and operating frequency 402
Supply of substrate bias voltage and operating frequency 405
Means of controlling substrate bias voltage and operating frequency 44

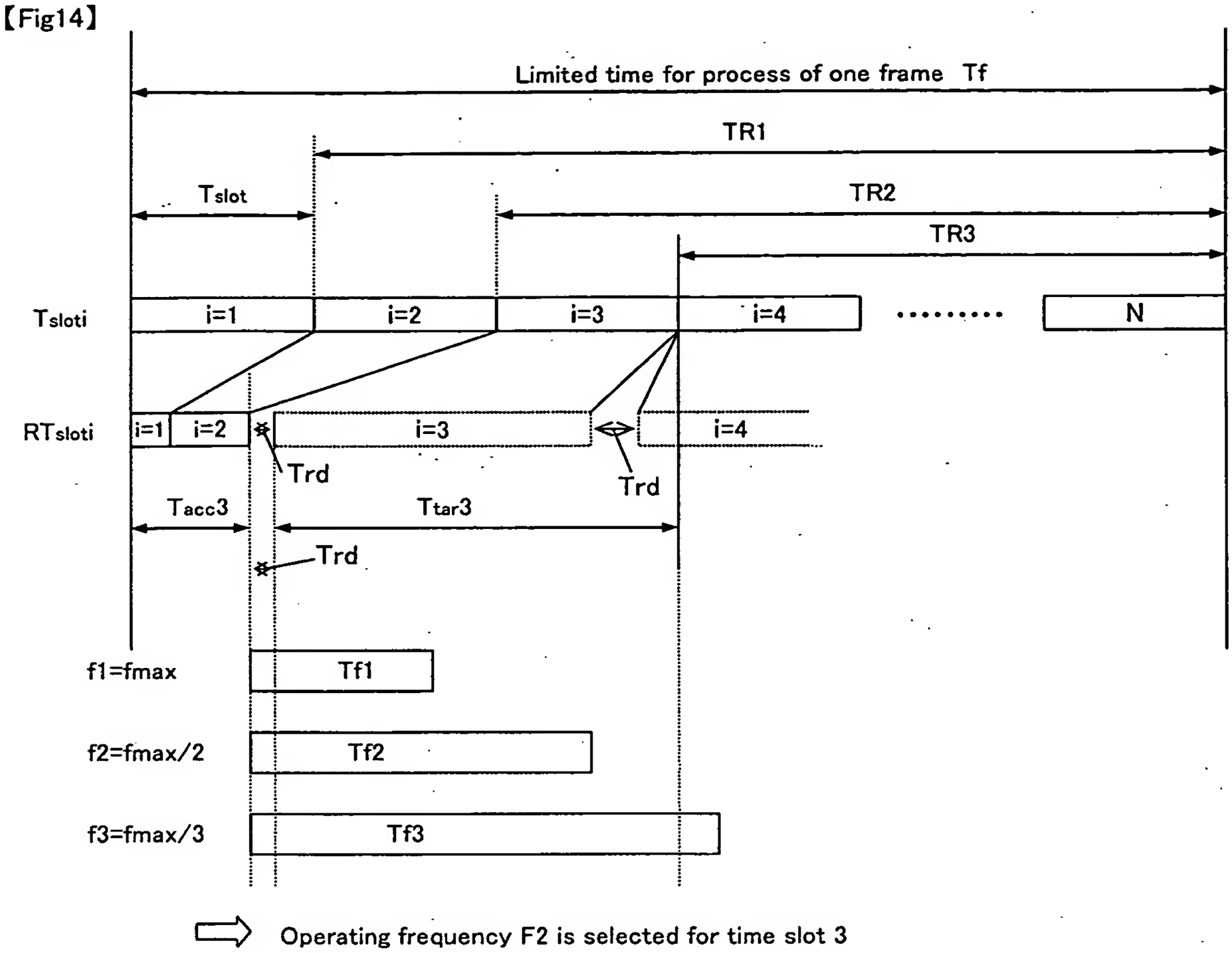
【Fig12】

Operating frequency (cycles／second)	Substrate bias voltage of n-channel MOS transistor (Vbn)	Substrate bias voltage of p-channel MOS transistor (Vbp)
f (1)	Vbn (1)	Vbp (1)
f (2) (>f (1))	Vbn (2)	Vbp (2)
f (3) (>f (2))	Vbn (3)	Vbp (3)
.	.	.
f (n) (>f (n−1))	Vbn (n)	Vbp (n)
.	.	.
f (r) (>f (r−1))	Vbn (r)	Vbp (r)

【Fig13】

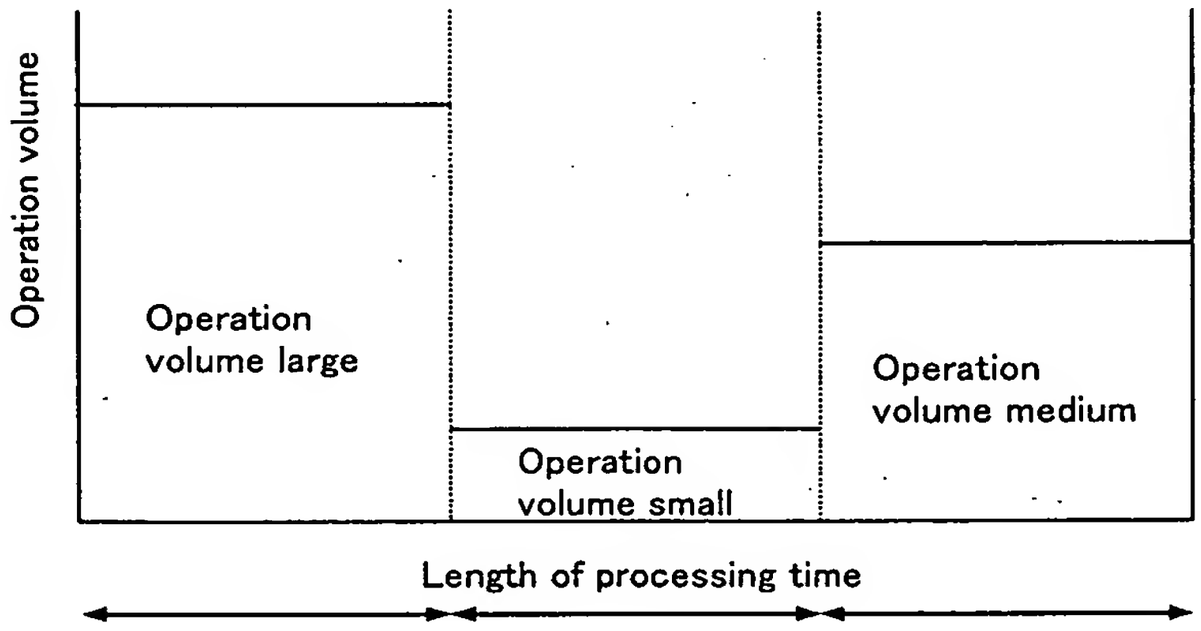
Operating frequency (cycles／second)	Power-supply voltage (VDD)	Substrate bias voltage of n-channel MOS transistor (Vbn)	Substrate bias voltage of p-channel MOS transistor (Vbp)
f (1)＝50	VDD(1)＝0.5	Vbn (1) = −1.0	Vbp (1) = 1.5
f (2)＝100	VDD(2)＝0.6	Vbn (2) = −0.4	Vbp (2) = 1.0
f (3)＝150	VDD(3)＝0.8	Vbn (3) = 0	Vbp (3) = 0.8
f (4)＝200	VDD(4)＝0.9	Vbn (4) = 0.2	Vbp (4) = 0.7
f (5)＝250	VDD(5)＝1.0	Vbn (5) = 0.5	Vbp (5) = 0.5

【Fig14】

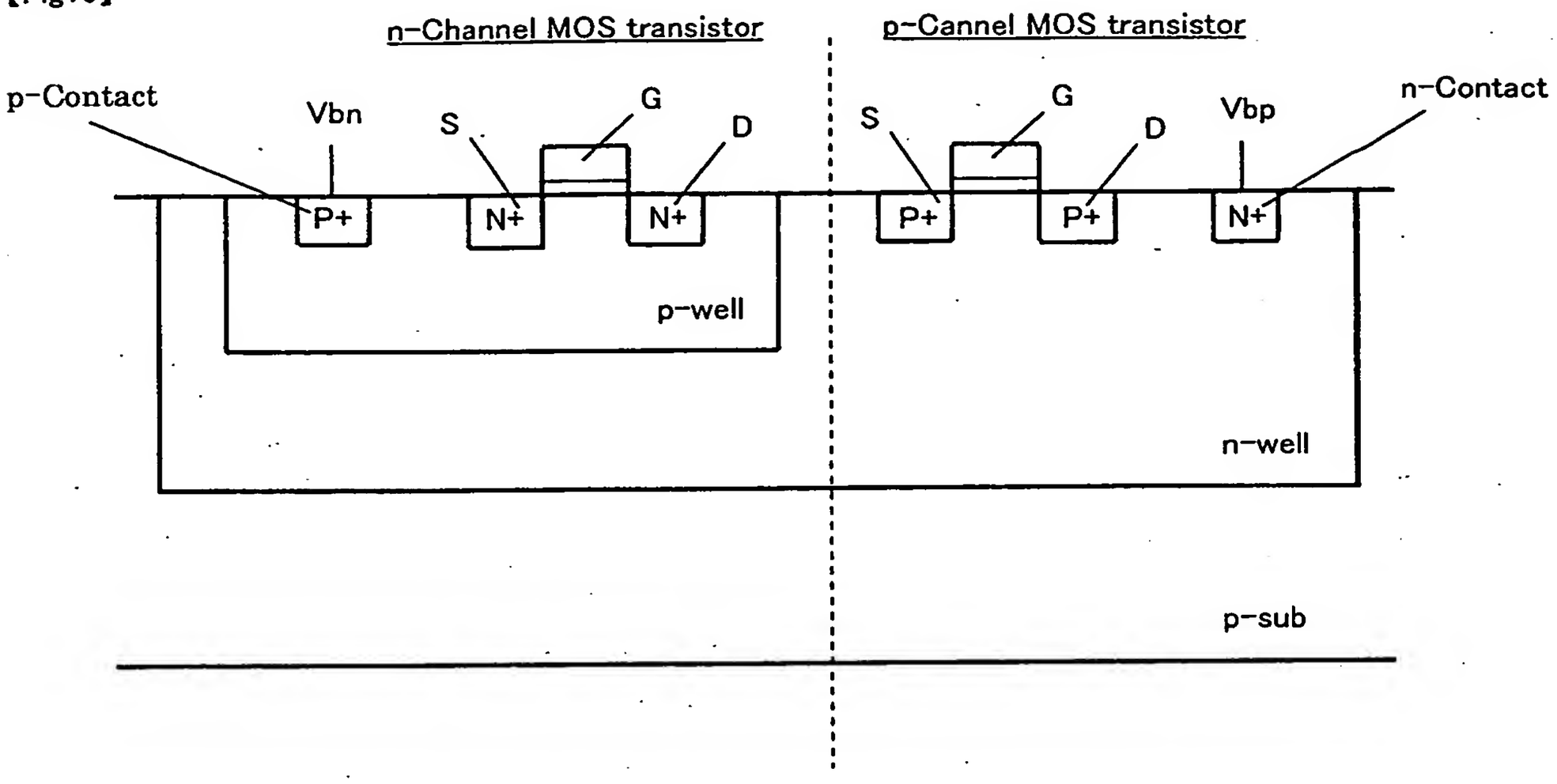


⇨ Operating frequency F2 is selected for time slot 3

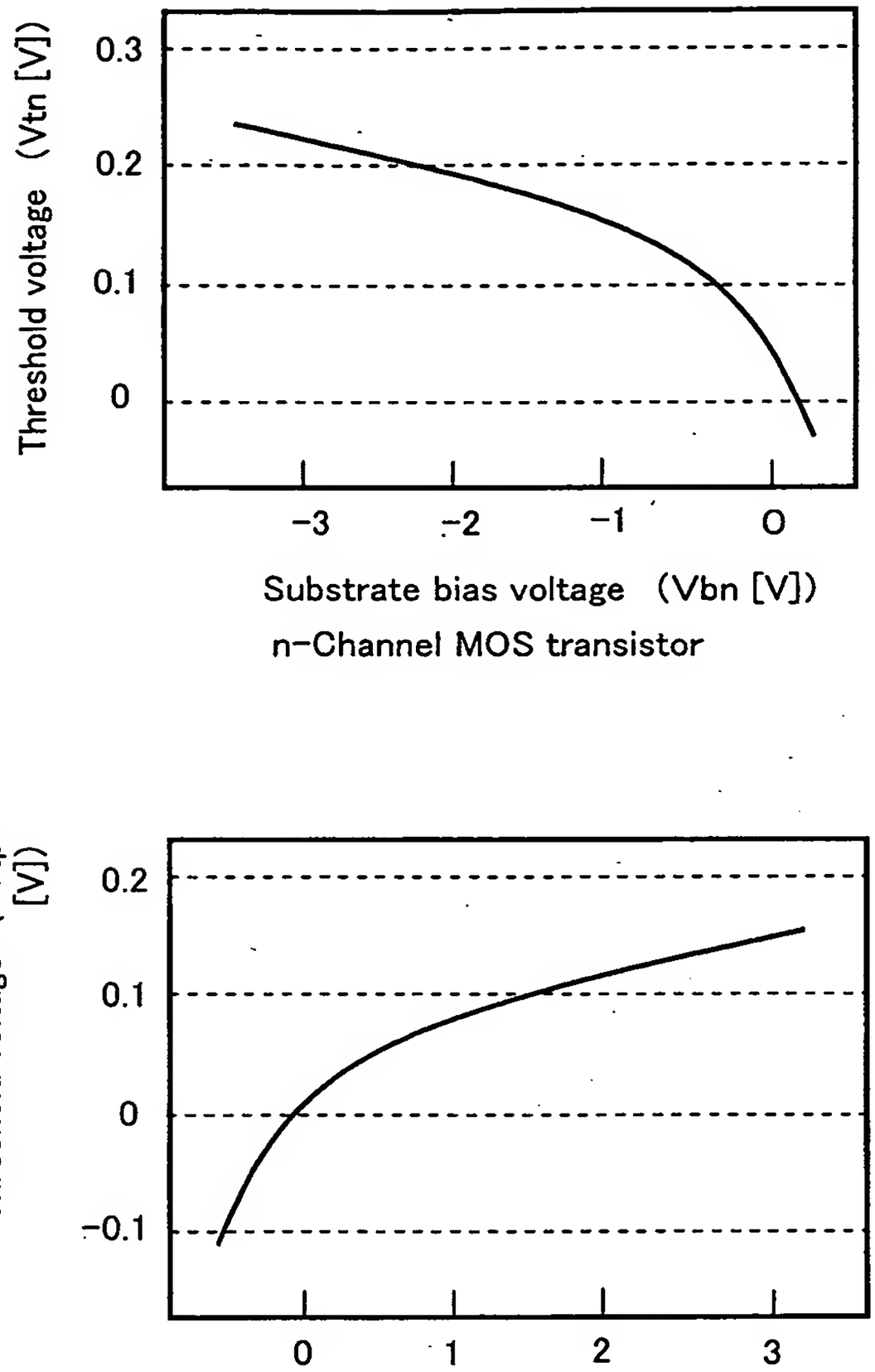
【Fig15】



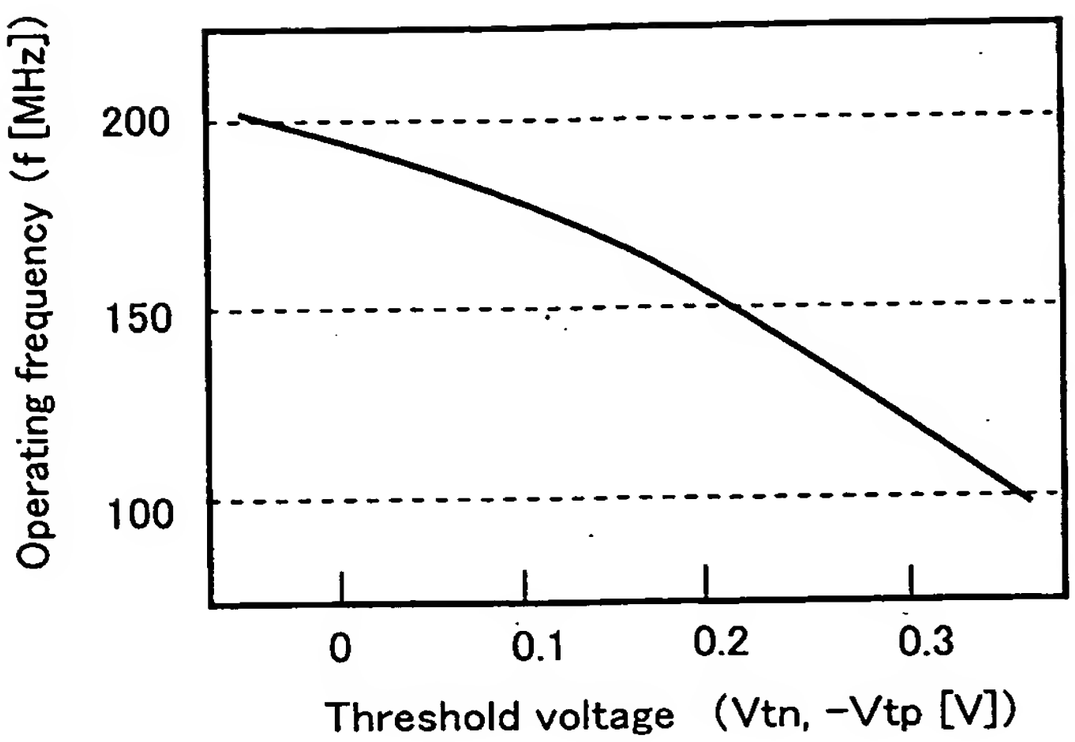
【Fig16】


n-Channel MOS transistor
p-Cannel MOS transistor
p-Contact
Vbn
S
G
D
S
G
D
Vbp
n-Contact
P+
N+
N+
P+
P+
N+
p-well
n-well
p-sub

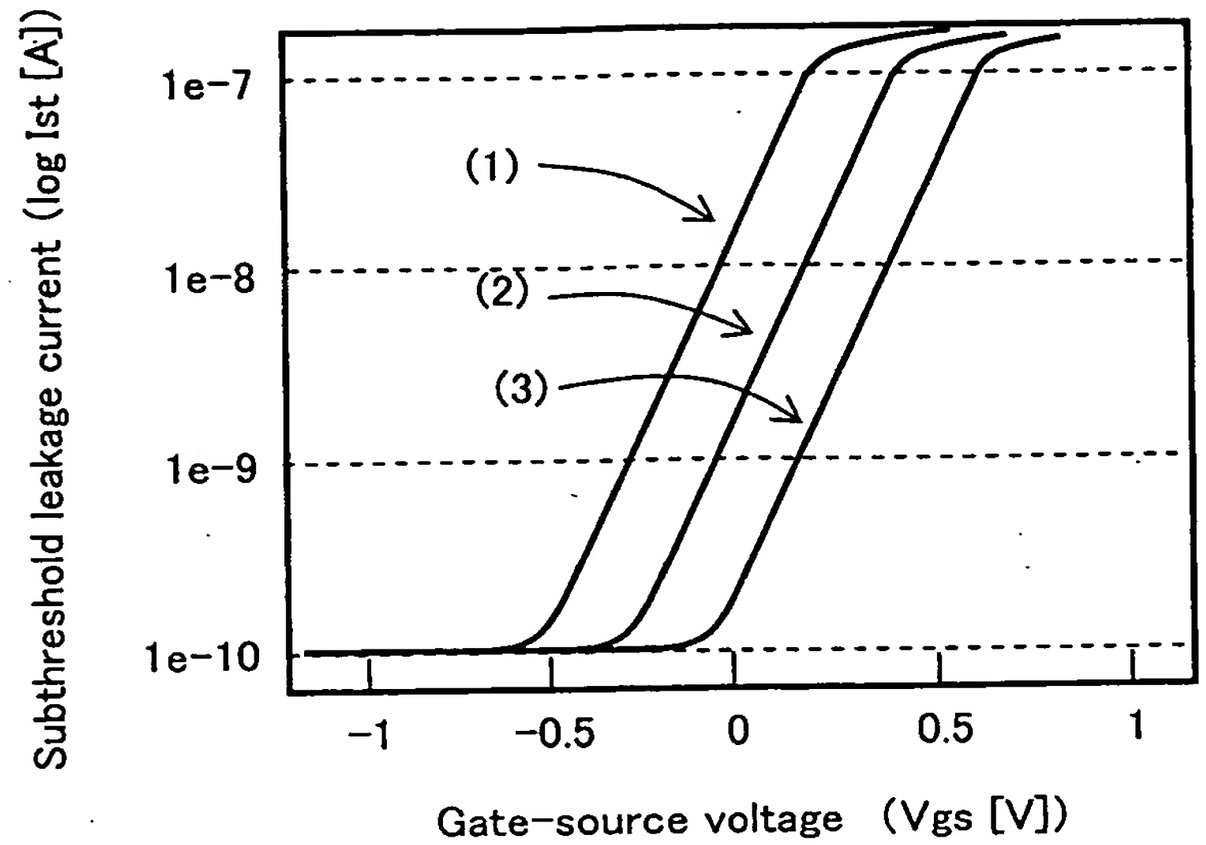
【Fig17】


Threshold voltage (Vtn [V])
0.3
0.2
0.1
0
−3
−2
−1
0
Substrate bias voltage (Vbn [V])
n−Channel MOS transistor
Threshold voltage (−Vtp [V])
0.2
0.1
0
−0.1
0
1
2
3
Substrate bias voltage (Vbp [V]) −Power−supply voltage (VDD [V])
p−Channel MOS transistor

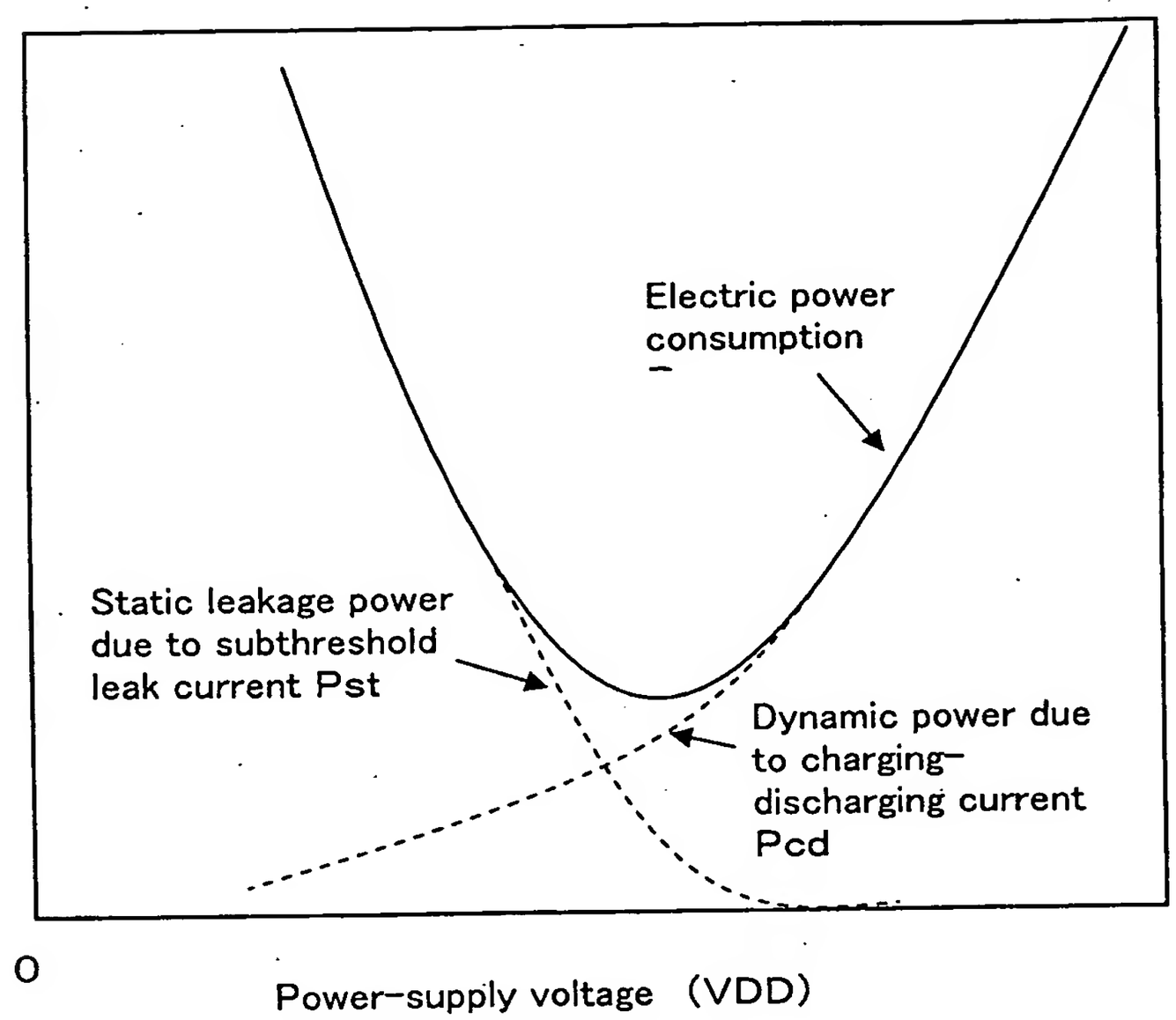
【Fig18】


Operating frequency (f [MHz])
200
150
100
0
0.1
0.2
0.3
Threshold voltage (Vtn, −Vtp [V])

【Fig19】


Subthreshold leakage current (log Ist [A])
1e-7
1e-8
1e-9
1e-10
(1)
(2)
(3)
-1
-0.5
0
0.5
1
Gate-source voltage (Vgs [V])

【Fig20】


Electric power consumtion (P)
Electric power consumption
Static leakage power due to subthreshold leak current Pst
Dynamic power due to charging–discharging current Pcd
0
Power–supply voltage (VDD)